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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,060	09/30/2003	Xiangfeng Duan	01-001420	1190

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EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,060	DUAN ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *173,175-222,224,225,227-243 and 245* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *173,175-222,224,225,227-243 and 245* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Allowable Subject Matter

1. Applicant is advised that the Notice of Allowance mailed March 22, 2005 is vacated. If the issue fee has already been paid, applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may wait until the application is either found allowable or held abandoned. If allowed, upon receipt of a new Notice of Allowance, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a specified Deposit Account.

2. The indicated allowability of claims 173, 175 – 222, 224, 225, 227 – 243, and 245 is withdrawn. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 173, 175 - 178, 180, 183 – 186, 193 - 197, 201, 202, 204 – 206, and 208 are rejected under 35 U.S.C. 102(b) as being anticipated by Frey (US Patent 5920078).

5. Frey teaches an electronic substrate (10) having a plurality of semiconductor devices, comprising:

a substrate (12);

a thin film of nanowires (18), deposited on said substrate, with a sufficient density of nanowires to achieve an operational current level, wherein said thin film of nanowires defines a plurality of semiconductor device regions (col. 4 lines 20 – 25); and

one or more pairs of source (20) and drain (21) contacts formed at said semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein at least two or more nanowires (fig. 3) within said thin film of nanowires form a channel between each of said respective pairs of source and drain contacts (col. 3 lines 55 – 58);

wherein at least a subset of the semiconductor devices comprises diodes, and wherein said one or more pairs of source and drain contacts comprise anode and cathode electrodes formed above or below said thin film of nanowires (fig. 5);

wherein said thin film of nanowires forms a p-n junction between said anode and cathode electrodes (fig. 5);

wherein said diodes comprise light emitting diodes (fig. 5);

wherein at least a subset of the semiconductor devices comprises logic devices; (col. 4 lines 25 – 28); and

wherein at least a subset of the semiconductor devices comprises an active matrix driving circuit (col. 4 lines 20 – 25).

6. Further comprising one or more gate electrodes (15) formed on the substrate, wherein said thin film of nanowires is formed on said one or more gate electrodes, and said one or more pairs of source and said drain contacts are formed on said thin film of nanowires (fig. 3);

wherein said one or more pairs of source and said drain contacts are formed on said substrate, said thin film of nanowires is formed on said source and said drain contacts, and further comprising one or more gate contacts formed on said thin film of nanowires (fig. 3);

wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said substrate, and said thin film of nanowires is formed on said one or more gate electrodes and said one or more pairs of source and drain contacts (fig. 3);

wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said thin film of nanowires (fig. 3);

wherein said channels comprise more than one nanowire (fig. 3);

wherein at least a subset of said gate electrodes comprise more than one thin film of nanowires (fig. 3);

wherein at least a subset of the channels comprises a p-n junction, whereby during operation the p-n junctions emit light (col. 3 lines 27 – 42);

wherein said nanowires are doped (col. 3 lines 27 – 42);

wherein at least a subset of said nanowires have doped cores (col. 3 lines 27 – 42);

wherein at least a subset of the semiconductor devices are electrically coupled to another circuit (col.4 lines 20 – 25); and

wherein at least a subset of the semiconductor devices are physically coupled to another circuit (col.4 lines 20 – 25).

7. Claims 173, 175, 181 – 187, 192 – 194, 196 – 201, 205, 219, 224, 225, 227 – 236, 239, 240, 242 – 243, and 245 are rejected under 35 U.S.C. 102(e) as being anticipated by Avouris et al. (USPAB 2002/0173083).

8. Avouris et al. teach an electronic substrate and a method of making thereof having a plurality of semiconductor devices, comprising:

deposited on a substrate a substrate a thin film of nanowires with a sufficient density of nanowires to achieve an operational current level (fig. 2B);

defining a plurality of semiconductor device regions in or on the thin film of nanowires (fig. 9B); and

forming one or more pairs of source and drain contacts at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein at least two or more nanowires within said thin film of nanowires form a channel between each of said respective pairs of source and drain contacts (figs. 2B, 9B);

wherein at least a subset of the semiconductor devices comprises diodes, and wherein said one or more pairs of source and drain contacts comprise anode and cathode electrodes formed above or below said thin film of nanowires (paragraph 47);

wherein said nanowires are aligned substantially parallel to their long axis (fig. 2B);

wherein the nanowires are aligned approximately parallel to an axis between the source and drain contacts (fig. 9A);

further comprising one or more gate electrodes formed on the substrate, wherein said thin film of nanowires is formed on said one or more gate electrodes, and said one or more pairs of source and said drain contacts are formed on said thin film of nanowires (fig. 7B);

wherein said one or more pairs of source and said drain contacts are formed on said substrate, said thin film of nanowires is formed on said source and said drain contacts, and further comprising one or more gate contacts formed on said thin film of nanowires (fig. 8);

wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said substrate, and said thin film of nanowires is formed on said one or more gate electrodes and said one or more pairs of source and drain contacts (fig. 7B);

wherein said one or more gate electrodes and said one or more pairs of source and drain contacts are formed on said thin film of nanowires (fig. 9A);

further comprising interconnects between a subset of the semiconductor devices (figs. 9);

wherein said channels comprise more than one nanowire (fig. 2B);

wherein at least a subset of the semiconductor devices are electrically coupled to another circuit (figs. 9);

wherein at least a subset of the semiconductor devices are physically coupled to another circuit (figs. 9);

further comprising a layer of oxide (918) deposited on at least a portion of said nanowires (figs. 9); and

further comprising at least one gate contact formed above or below said plurality of nanowires (figs. 7B, 9A).

wherein the plurality of nanowires comprises at least five or more nanowires (fig. 2B).

wherein the plurality of nanowires have a sufficient density to provide an operational current level of at least about 10 nanoamps (paragraphs 39, 44);

wherein at least one of said one or more shell layers comprises an oxidized shell layer to thereby form a gate dielectric about said core (paragraph 53);

wherein said nanowires are doped (paragraph 21); and

wherein at least a subset of said nanowires have doped cores and shells (fig. 2A, & paragraph 21).

9. Claims 173, 179, 191, 209 – 214, 218, and 220 are rejected under 35 U.S.C. 102(e) as being anticipated by Skarupo et al. (US Patent 6438025).

10. Skarupo et al. teach an electronic substrate and a method of making thereof having a plurality of semiconductor devices (figs. 3 – 6), comprising:

deposited on a substrate (fig. 3) a thin film of nanowires with a sufficient density of nanowires to achieve an operational current level (col. 7 lines 50 – 62);

defining a plurality of semiconductor device regions in or on the thin film of nanowires (fig. 5); and

forming one or more pairs of source (24) and drain (26) contacts at the semiconductor device regions to thereby provide electrical connectivity to the plurality of semiconductor devices, wherein at least two or more nanowires within said thin film of nanowires form a channel between each of said respective pairs of source and drain contacts (col. 9 lines 14 – 21);

wherein the circuit is a memory circuit (col. 15 lines 56 – 67);

wherein the patterned nanowires are photolithography patterned (col. 9 lines 14 – 21);

wherein the nanowires are single crystal nanowires (col. 10 lines 15 – 50), and wherein electric carriers transport through said single crystal nanowires with a mobility comparable to that of electric carriers transporting in a device formed from traditional planer single crystal semiconductor materials (col. 14 line 66 – col. 15 line 6);

wherein said nanowires comprise sufficient density to have statistic probability of achieving a device anywhere on the substrate (col. 11 lines 35 – 44); and

wherein the nanowires are ballistic conductors having a mobility greater than that of a single crystal semiconductor material (col. 15 lines 1 – 6)

11. Regarding claims 210 – 214 the method of forming the device does not further structurally distinguish the resultant device itself. Therefore, these limitations have not been given any patentable weight.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 203, and 207 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avouris et al. (USPAB 2002/0173083) in view of Skarupo (US Patent 6438025).

15. Avouris et al. teach the features previously outlined, but lack wherein the circuit is a memory circuit.

16. However, Skarupo teaches a device wherein the circuit is a memory circuit (col. 15 lines 56 – 67) for increased readout speed and narrowing effective track width (col. 3 lines 44 – 60) and

17. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Skarupo into the Avouris et al. reference to form a memory device with increased readout speed.

18. Claims 188, 189, 190, 209, and 215 – 217, 221, 222, 237, 238 and 241 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avouris et al. (USPAB 2002/0173083) in view of Lieber et al. (USPAB 2002/0117659).

19. Avouris et al. teach the features previously outlined, but lack:

wherein said substrate comprises a flexible material;

wherein said substrate comprises transparent material;

wherein the nanowires are mechanically aligned;

wherein the nanowires are flow-aligned;

wherein the nanowires are shear-force aligned;

wherein the nanowires are randomly oriented;

wherein the nanowires are formed as a monolayer film, a sub monolayer film or a multilayer film; and

wherein the plurality of nanowires comprises at least 100 or more nanowires.

20. However, Lieber et al. teach nanowires:

wherein said substrate comprises a flexible material (paragraph 134);

wherein said substrate comprises transparent material (paragraph 134);

wherein the nanowires are mechanically aligned (paragraph 121);

wherein the nanowires are flow-aligned (paragraph 123);

wherein the nanowires are shear-force aligned (paragraph 124);

wherein the nanowires are randomly oriented (paragraph 132);

wherein the nanowires are formed as a monolayer film, a sub monolayer film or a multilayer film (paragraph 125); and

wherein the nanowires comprise a plurality (paragraph 132).

21. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the deposition teachings of Lieber et al. into the Avouris et al. reference for optimization, where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art.

22. Art made of record and not relied upon, considered pertinent to applicant's disclosure include Smirnov et al. (US patent 6274007), Fonash et al. (USPAB 2004/0005258), Zhang et al. (US Patent 2004/0036128), Kern et al. (USPAB 2004/0031975), Brown et al. (UPAB 2005/0064618), and Jacobsen et al. (US Patent 6815218).

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2891

IA

August 21, 2005

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER